Cascaded Multilevel PV Inverter With Improved Harmonic Performance During Power Imbalance Between Power Cells

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***Abstract*—The difference in power cell irradiances in cascaded multilevel converters results in different duty cycles among those cells when maintaining the maximum power point tracking (MPPT). However, the difference in cell duty cycles is undesired since it is proportional to the output voltage and current distortions. To this regard, a multilevel topology for photovoltaic (PV) applications is proposed, where an H6 bridge power cell is used instead of an H-bridge one. In case of solar irradiance mismatch among the power cells, the proposed converter injects power with lower voltage from the shaded cells without altering the PV voltage; hence maintaining the MPPT operation. This modification allows us to retain an equal duty cycle in all the power cells whatever the meteorological conditions are present; consequently, maintaining good output voltage and current waveform qualities. To test the effectiveness of the proposed solution, a detailed simulation model as well as an experimental prototype is built. The obtained results show that the proposed topology provides significantly improved output voltage and current qualities compared to the cascaded H-bridge one. The performance of the proposed topology compared to one offering improved harmonics performance, according to the European efficiency, has been also compared, where an enhancement of 2.64% has been registered.**

***Index Terms*—Cascaded converter, grid connected, H-bridge, maximum power point tracking (MPPT), modular multilevel converter (MMC), partial shading, perturb and observe, photovoltaic (PV), power quality.**

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I. INTRODUCTION

MULTILEVEL converters (MLCs) are very promising candidate power electronic converters since they offer a robust, efficient, and fault-tolerant features [1]–[3]. These power converter topologies are able to output high-quality voltage waveforms with power switches operating at even the fundamental frequency when the number of levels is high enough. One the other hand, the high-quality voltage allows the use of less sizable output filter [4]. Among them is the cascaded H-bridge (CHB) converter topology [5], which consists of series-connected H-bridges, each of which is fed by a separate dc voltage source. This characteristic makes it possible to connect PV panels in each H-bridge; thus, achieving independent maximum power point tracking (MPPT), which in turn, improves the efficiency of the overall system and increases the energy injected to the grid [6].

The commonly used pulsewidth modulation (PWM) strategy in MLCs is the phase shifted PWM (PS-PWM) [7]. The PS-PWM in CHB application is described as multi-unipolar carriers, one carrier designated for each H-bridge, where these carriers are shifted by T_s/n with respect to one another. Here, T_s is the carriers period, and n is the number of H-bridges. Equal power distribution and equal power losses among the power cells, as well as multiplicative effect $(2\mathrm{nm}_f)$ in the converter output voltage switching frequency, are offered when using this modulation technique [7].

However, in case the power cells are subjected to uneven solar irradiance due to dust on the PV panels or partial shading, the system would be unbalanced. This imbalance can be grouped into two categories, interphase imbalance and intraphase imbalance. The former is believed to be an old existing problem, which is similar to any interphase imbalance issue, for which there are hundreds of solutions in the literature [8]. Nevertheless, there have been new solutions introduced, where MLCs is their application [9], [10]. The intraphase imbalance, however, is a contemporary problem that came as a challenge with MLCs.

The main causes of the harmonics generated in the converter output signals when the solar irradiation is not equal over the power cells are the difference in cell duty cycles and dc-link voltages. The controller limits the duty cycle in the shaded

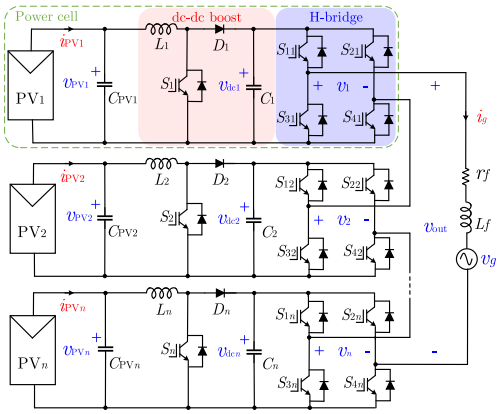

Fig. 1. Classical dc–dc boost + H-bridge-based power cell MLC (CHBB).

power cell in order to match its new MPP current when the solar irradiance decreases; consequently, the modulator receives different duty cycles. In this case, the shaded power cell starts injecting power by some delay (T_D) and stops injecting it before the supposed time by T_D. However, in MLCs, the cells are grouped together to form the converter output signals (output current and voltage), and the timing is a critical parameter, i.e., any advanced or delayed operation of any power cell compared to the supposed timing may deteriorate the output signals.

Several attempts to mitigate this problem are reported in the literature [11]–[15]. In [11], variable switching angles is the main operation principle, where this strategy offers a cheap solution; however, it is valid only when $n = 3$ due to the complex computation required. Furthermore, during sever partial shadings, changing the carrier shift angles does not improve the output signals quality to an acceptable level. Marquez *et al.* [12] proposed the employment of an extra battery-fed power cell to overcome this problem in case $n = 2$. A dc–dc boost converter has been added into each power cell in [13], as shown in Fig. 1 (referred to as CHBB thereafter), where a modified modulation strategy is proposed to keep the energy among the dc-link capacitors at a similar level; hence, operating all the cells at similar duty cycles. Modular cascaded multilevel quasi-*Z*-source inverter offers flexibility in the power quality matter as the H-bridges' voltages are independent on the PV voltages—only some changes on its modulation and control are required, as elaborated in [14]. The operation of a solid-state transformer-based power cell in a star-connected CHB in the presence of both interphase and intraphase imbalances is studied in [15]. The previously mentioned topology-based solutions incorporate a lot of active and passive components—especially inductors—in the power cells, and in some cases, higher switching frequency is required, which not only increases the size, weight, and cost of the converter, but also degrades the system's overall efficiency.

In this article, an H6 power cell based MLC is proposed, where the issue of the difference in duty cycles is disclosed. Note that, this article is an extension of [16], where more theoretical analyses of the harmonics generated in an MLC in case of unbalanced power cells as well as experimental results are added. This article is organized as the following. Section II analyses the partial shading in the conventional CHB and the main factors behind the output voltage and current distortions under such case. The proposed topology is presented in Section III. Section IV shows the control approach adopted for operating the proposed converter, as well as the developed modulation for the added switches. Section V compares between the proposed and the previously introduced solutions aimed into mitigating from the harmonics content during partial shading. Simulation and experimental evaluation tests are shown and discussed in Sections VI and VII, respectively. Section VIII concludes this article.

II. Analysis of the Partial Shading in the Conventional CHB Topology

Fourier expansion is one of the most straightforward and sufficiently accurate tools in signal processing [17], which is thus, going to be used in this article to analyze the converters' output signals quality. According to the Fourier hypothesis, any periodic function *f*(*t*) can be expressed as a dc offset plus a sum of sines and cosines as the following:

$$f(t) = c_0 + \sum_{h=1}^{\infty} \left[a_h \cos\left(h\omega t\right) + b_h \sin\left(h\omega t\right)\right] \tag{1}$$

where ω is the smallest angular frequency to be evaluated. The coefficients a_h and b_h are defined as follows:

$$\begin{aligned} a_h &= \frac{1}{\pi}\int_0^{2\pi} f(t)\cos\left(h\omega t\right) d\left(h\omega t\right) \\ b_h &= \frac{1}{\pi}\int_0^{2\pi} f(t)\sin\left(h\omega t\right) d\left(h\omega t\right). \end{aligned} \tag{2}$$

In this article, the function to be analyzed is the converter's output voltage, which is the sum of all power cell voltages. The *i*th power cell output voltage is considered as a square pulse train with a variable duty cycle, which can be expressed as

$$v_i(t) = v_{\mathrm{dc}i} D_i, \quad \text{where } i = 1, \ldots, n \tag{3}$$

such as D_i and $v_{\mathrm{dc}i}$ are the duty cycle and voltage in the *i*th power cell. Fourier expansion of each power cell's output voltage can be then expressed as follows:

$$v_i(t) = c_{0i} + \sum_{h=1}^{\infty} \left[a_{hi} \cos\left(h\omega_c t\right) + b_{hi} \sin\left(h\omega_c t\right)\right] \tag{4}$$

where ω_c is the carrier angular frequency.

The solution can be simplified by nulling b_{hi} on the assumption that the time origin is chosen in a way the function $v_i(t)$ shows an even symmetry. In this way, Fourier coefficients can be found as follows:

$$\begin{aligned} c_{hi} &= \frac{1}{\pi}\int_0^{D_i\pi} v_i(t)\, d\left(\omega_c t\right) = v_{\mathrm{dc}i} D_i \\ a_{hi} &= \frac{2}{\pi}\int_0^{D_i\pi} v_i(t)\cos\left(h\omega_c t\right) d\left(\omega_c t\right) = \frac{2v_{\mathrm{dc}i}}{h\pi}\sin\left(h\pi D_i\right). \end{aligned} \tag{5}$$

The output voltage of the ith power cell in Fourier expansion form can be then written as follows:

$$v_i(t) = v_{\mathrm{dc}i}D_i + \sum_{h=1}^{\infty} \frac{2v_{\mathrm{dc}i}}{h\pi} \sin\left(h\pi D_i\right) \cos\left(h\omega_c t\right) \tag{6}$$

Thus, the total output voltage can be described as

$$v_{out}(t) = \sum_{i=1}^{n} \left(v_{\mathrm{dc}i}D_i + \sum_{h=1}^{\infty} \frac{2v_{\mathrm{dc}i}}{h\pi} \sin(h\pi D_i) \cos\left(h\omega_c t + \theta_i\right) \right) \tag{7}$$

where θ_i is the ith carrier shift angle, which is estimated as

$$\theta_i = \frac{2\pi}{n}\left(i-1\right). \tag{8}$$

As it can be seen from (7), the hth harmonic content at the total output voltage is expressed as follows:

$$v^h = \sum_{i=1}^{n} \frac{2v_{\mathrm{dc}i}}{h\pi} \sin\left(h\pi D_i\right) \cos\left(h\omega_c t + \theta_i\right). \tag{9}$$

If the converter is assumed to have three power cells, the hth harmonic content would be written as in the following:

$$\begin{aligned} v^h = {} & \frac{2v_{\mathrm{dc}1}}{h\pi} \sin\left(h\pi D_1\right) \cos\left(h\omega_c t\right) \\ & + \frac{2v_{\mathrm{dc}2}}{h\pi} \sin\left(h\pi D_2\right) \cos\left(h\omega_c t + \frac{2\pi}{3}\right) \\ & + \frac{2v_{\mathrm{dc}3}}{h\pi} \sin\left(h\pi D_3\right) \cos\left(h\omega_c t + \frac{4\pi}{3}\right). \end{aligned} \tag{10}$$

From (10), in order for the hth harmonic content to be eliminated in the total output voltage, the dc-link voltages, as well as the duty cycles have to be equal. In case of partial shading, the control would decrease the duty cycle of the shaded power cell in order for its current to be limited to a lower level according to the partial shading severity.

An illustrative example has been performed and is shown in this article to further clarify the mathematical derivations' outcome. Fig. 2 shows test cases of balanced and unbalanced CHB operations. As it can be seen from plot (cz) of this figure, as the third cell get shaded, its duty cycle decreases causing the cell to start injecting power with a delay T_D with respect to the supposed time, and stopping before the supposed time by a T_D. This duty cycle decrease causes some pulses to be thinner or even completely absent from the total output voltage, yielding into a distortion in the latter, as highlighted in the zoomed-in view [see plot (dz)]. It is also noteworthy that the effective switching frequency reduces due to those absent pulses as shown in Fig. 2(d2).

III. Proposed Multilevel Topology

As described by (10), an alternative to eliminate the hth harmonic content during partial shading is either by equalizing all cells duty cycles and voltages or by increasing all cells duty cycle peaks to be close to unity. In order to rise the duty cycle of the shaded power cell back to a value that is close to the unity, the cell output voltage has to be decreased; however, the point

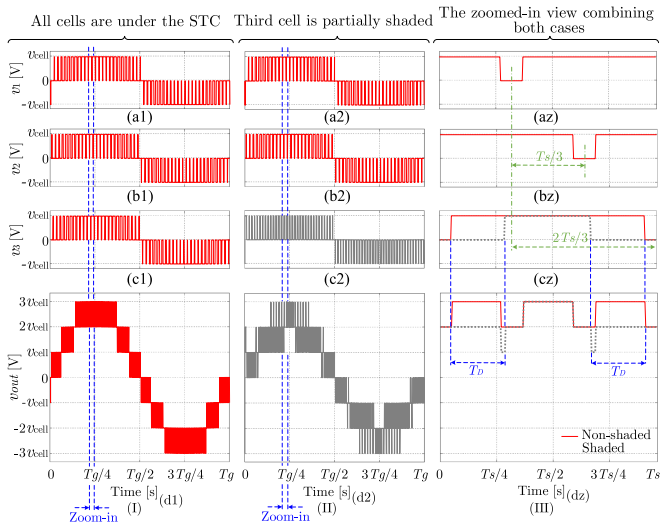

Fig. 2. Each power cell's output voltage in addition to the resulted total output voltage, in both cases, balanced, and unbalanced solar irradiance among the cells.

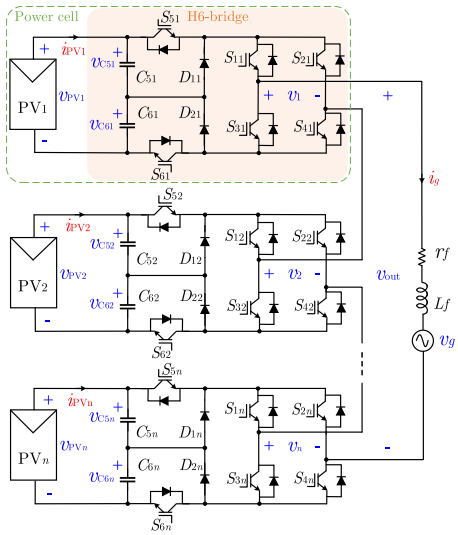

Fig. 3. Proposed cascaded multilevel topology for PV systems.

is to not alter the PV voltage and MPPT. A dc–dc stage can be employed between each H-bridge and PV string, ensuring a decoupled voltage between the H-bridge's dc link and PV string. The dc–dc converter can be a boost [13] (see Fig. 1), buck—boost [18], or flyback [19]. However, this solution adds more inductors; consequently, the hardware is more expensive and sizable. Furthermore, the dc–dc stages operate at higher switching frequency, affecting the efficiency of the system negatively. For this purpose, it is proposed in this article to replace the H-bridge in each power cell by an H6 one, where the dc-link capacitor is substituted by a split one, and only two active semiconductor devices and two diodes are added. The overall schematic diagram of the proposed MLC for PV applications, where n cells are regarded, is depicted in Fig. 3. The proposed concept comprises injecting power from the shaded power cell

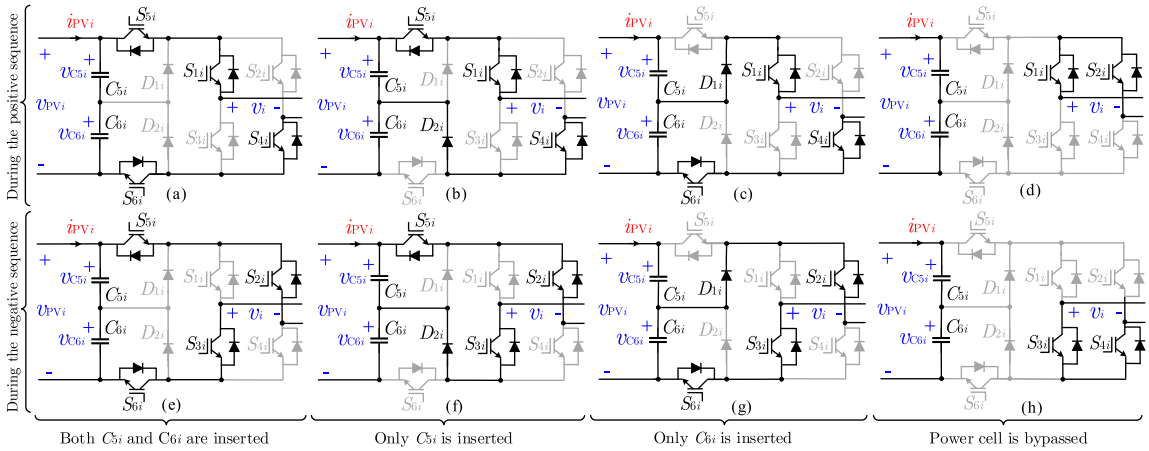

Fig. 4. Operation states in the proposed power cell.

with less voltage, without altering the PV string voltage (see Fig. 4); hence, retaining the MPPT.

Each cell's output voltage can be determined as the follows:

$$v_i = (S_{1i} - S_{2i})\,(S_{5i} v_{C5i} + S_{6i} v_{C6i}) \tag{11}$$

where *Sxi* is the *xi* active semiconductor state, which could be either ON or OFF. According to Fig. 3, i refers to the cell's index and x refers to the semiconductor number in that cell. The variables v_i, v_{C5i}, and v_{C6i} are, respectively, the output voltage, the voltage at the terminals of capacitor C_5, and the voltage at the terminals of capacitor C_6 of the ith cell.

If the capacitors charge in each power cell is well balanced, the cell's output voltage can be expressed as

$$v_i = v_{\mathrm{PV}i}\,(S_{1i} - S_{2i})\left(\frac{S_{5i} + S_{6i}}{2}\right) \tag{12}$$

such as $v_{\mathrm{PV}i}$ is the voltage at the terminals of the ith PV string.

The dynamic behavior of each power cell can be described by the following differential equation:

$$C_{\{5,6\}i}\frac{dv_{C\{5,6\}i}}{dt} = \left(i_{\mathrm{PV}i} - (S_{1i} - S_{2i})\,S_{\{5,6\}i}\,i_g\right). \tag{13}$$

Thus, according to Kirchhoff's voltage law, the overall system's dynamic behavior can be assessed as in the following equation:

$$L_f\frac{di_g}{dt} = \sum_{i=1}^{n}\left((S_{1i} - S_{2i})\left(\frac{S_{5i} + S_{6i}}{2}\right)v_{\mathrm{PV}i}\right) - r_f\,i_g - v_g \tag{14}$$

where i_g, v_g, L_f, and r_f are, respectively, the grid current, grid voltage, filter inductance, and filter internal resistor.

IV. Control Structure in the Proposed Converter

The control of the proposed topology is divided into three parts, grid injected current control, an independent MPP tracking in each cell, and H6 capacitors insertion and voltage balancing control.

The classical control, with one proportional integral (PI) controller for each cell voltage and one proportional resonant (PR) controller for the output current is adopted in this article (see Fig. 5) [6]. This control strategy has proven to be one of the most efficient techniques when using different voltages in the cells, which is the case here since these voltages will be determined by using separate MPP trackers [6]. As can be seen from Fig. 5, from $i = 2$ to n, the cell voltages are the only controlled variables in the loops. The voltages are controlled through PI controllers, which their outputs provide the modulation indices. These PI controllers can be expressed as the following:

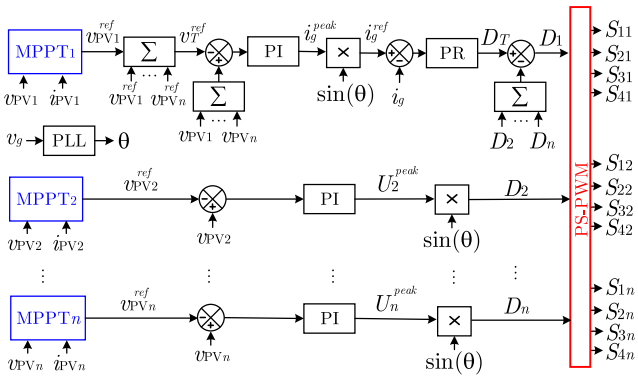

Fig. 5. Control structure adopted for the proposed cascaded H6 converter.

$$D_i^{\mathrm{peak}} = K_P^v\left(v_{\mathrm{PV}i} - v_{\mathrm{PV}i}^{\mathrm{ref}}\right) + \frac{K_I^v}{s}\left(v_{\mathrm{PV}i} - v_{\mathrm{PV}i}^{\mathrm{ref}}\right) \tag{15}$$

where K_P^v and K_I^v are the proportional and integral gains of the cell voltage loop, respectively, and D_i^{peak} is the modulation index of the ith cell. In order to obtain the duty cycles, these modulation indices are multiplied by a normalized sinusoidal signal that is synchronized with the grid voltage. The phase angle of that latter is determined through a phase-locked loop.

In the first cell, one PI controller is designated to control the total voltage based on all the voltage references provided by the MPPTs. The output of this controller generates the grid peak current (i_g^{peak}), which is multiplied by a unitary sinusoidal signal that is synchronized with the grid voltage. The total voltage

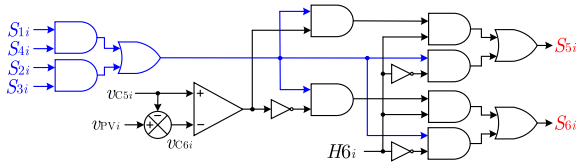

Fig. 6. Capacitors insertion and balancing in the partially shaded power cells.

regulator can be written as follows:

$$i_g^{\text{peak}} = K_P^V \sum_{i=1}^{n} v_{\text{PV}i} - v_{PVi}^{\text{ref}} + \frac{K_I^V}{s} \sum_{i=1}^{n} v_{\text{PV}i} - v_{\text{PV}i}^{\text{ref}} \quad (16)$$

such as K_P^V and K_I^V are the proportional and integral gains of the total voltage regulation loop, respectively.

A PR controller caters the reference to the modulator, which should be applied in order to obtain the grid current reference. The ideal PR controller is given by

$$D_T = K_P^I \left(i_g - i_g^{\text{ref}}\right) + \frac{K_R^I \left(i_g - i_g^{\text{ref}}\right) s}{s^2 + {\omega_g}^2} \quad (17)$$

where K_P^I and K_R^I are the proportional and resonant gains of the grid current controller, and ω_g is the grid angular frequency. However, the ideal PR controller may cause instability problems due to the infinite resonant gain. The latter problem can be solved by introducing a damping as follows:

$$D_T = K_P^I \left(i_g - i_g^{\text{ref}}\right) + \frac{2\omega_0 K_R^I \left(i_g - i_g^{\text{ref}}\right) s}{s^2 + 2\omega_0 s + {\omega_g}^2} \quad (18)$$

such as ω_0 represents the bandwidth around the grid frequency. Since D_T represents the total duty cycle, the duty cycle of the first cell is assessed by subtracting the sum of the rest of the switching functions from D_T

$$D_1 = D_T - \sum_{i=2}^{n} D_i. \quad (19)$$

The switching states of the H-bridges (*Sxi,* where $x \in$[1,4]), are generated from PS-PWM, whereas the added switches (*Sxi,* where $x \in$[5,6]) are generated as described in Fig. 6. These latter two switches are turned ON together in case the irradiance is balanced among all the cells and the corresponding cell is inserted. If the corresponding cell is shaded, these two switches are gated in a different manner. The switch corresponding to the more charged capacitor is turned ON when the power cell is inserted, i.e., if v_{C5i} is higher, then S_{5i} is turned ON when the cell is inserted, otherwise, S_{6i} is turned ON. In this way, the capacitors charge is balanced. Note that, H6$_i$ in Fig. 6 specifies whether the *i*th cell is shaded or not; it takes low logic value when nonshaded and high logic value otherwise. For assessing H6$_i$, the flowchart in Fig. 7 has been implemented, which takes into account both the high-order harmonics level and power unbalance. For the high-order harmonics, the 38th and 42nd have been selected, as they are the first to appear starting from $100 \times (1 - \delta)\%$ of unbalance. δ can be determined through empirical tests, as it changes based upon the employed number of levels, output filter size, and switching frequency.

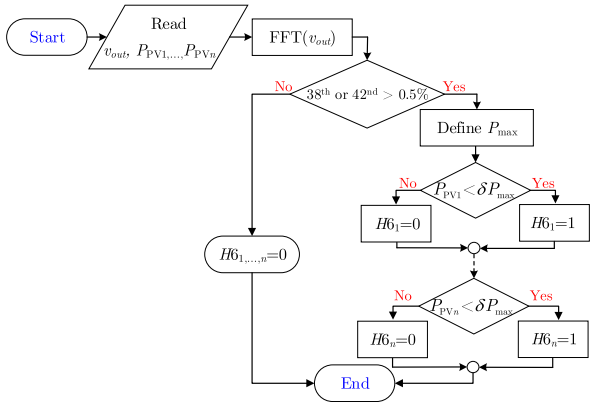

Fig. 7. Flowchart of the employed algorithm for defining the partially shaded power cell(s).

V. Comparison of the Proposed Topology With Its Counterparts

Table I compares the proposed converter with the topologies offering improved harmonic performance during partial shading among the cells, in terms of passives, active power switches, switching frequency, and control complexity. As it can be seen from this table, both the impedance source (IS) power cells use two inductors in each cell, whereas the CHBB power cell uses one. The proposed converter, however, does not use any. In terms of capacitors, the IS power cells are again the ones employing higher count. Furthermore, the IS power cells use some capacitors with high voltage rating, which is equal to the total cell voltage. The CHBB-based power cell uses the same capacitors count as in the proposed topology; however, one of them operates at the total cell voltage. It can be seen from Table I that the proposed topology employs the highest switches count compared to its counterparts. Nevertheless, the switches voltage in the proposed cascaded H6 are half the ones in the other topologies during partial shading. One can see from Table I that the proposed converter operates at the lowest switching frequency, being the CHBB the one requiring the highest. The switching frequency on the boost side can be diminished; however, this would be at the expense of the employed inductor size. The switching frequency in the IS power cells is lower than the one in the CHBB since two inductors are employed; but, all switches operate at this frequency, which is still higher than the one in the proposed converter. Both the switching and conduction losses will be compared in Section VI. On the control complexity aspect, the IS power cell based MLCs are the complex ones since the double stage functionality is merged into one, and the control of all inductor currents and capacitor voltages are performed from the same switches. The CHBB is simpler to control as the PV voltage/current is controlled independently by the dc–dc boost switch. The proposed topology is considered to be the simplest to be controlled as the same control algorithms adopted for the CHB can be used, with the exception of adding a simple algorithm for balancing the capacitor C_{5i} and C_{6i} voltages as shown in Section IV.

TABLE I
COMPARATIVE TABLE OF THE PROPOSED TOPOLOGY WITH ITS COUNTERPARTS CONVERTERS

	Passive components			Active power switches		Switching frequency	Control complexity
	Inductors	Capacitors		Count	Voltage rating		
		Count	Voltage rating				
DC-DC boost converter + H-bridge-based power cells	× 1	✓ 2	× One v_{dc} & one ≤ v_{dc}	✓ 5	$Si^1 \rightarrow < v_{dc}$ $Sxi,\ x \in [1,4] \rightarrow v_{dc}$	× $Si \rightarrow$high[2] $Sxi,\ x \in [1,4] \rightarrow$low	× Medium
Z-source converter-based power cells	× 2	× 3	× Two v_{dc} & one ≤ v_{dc}	✓ 4	All v_{dc}	× All Medium	× High
Quasi Z-source converter-based power cells	× 2	× 3	× One v_{dc} & two ≤ v_{dc}	✓ 4	All v_{dc}	× All Medium	× High
Proposed topology	✓ -	✓ 2	✓ Two $v_{dc}/2$	× 6	All v_{dc}	✓ All Low	✓ Low

[1]The index i is considered to be fixed to a number between 1 and n.
[2]The switching frequency ranges are considered to be classified here as: high when above 20 kHz, medium when within 8–20 kHz, and low when below 8 kHz.

VI. SIMULATION RESULTS

A. System Specifications

For the sake of validating the proposal experimentally, it has been modeled and simulated in details in PLECS [21], as a 1-kW single-phase inverter. The designed inverter is fed from PV strings, whose voltage range is from 120 to 190 V, and paralleled to 2 mF capacitors, in each cell. The PV panel parameters were taken from the datasheet of real ones, which are from Alfasolar GmbH, SI S21-170.A1 model. These PV panels have the following specifications: $v_{\mathrm{OC}} = 96$ V, $v_{\mathrm{MPP}} = 76$ V, $i_{\mathrm{SC}} = 2.83$ A, and $i_{\mathrm{MPP}} = 2.2$ A under the standard test conditions (STC). In order to reach the desired voltage level acquiescing to grid connection, two PV panels of those were simulated to be connected in series in each cell, where the cells count is three. The grid fundamental magnitude and angular frequency have been set to $\sqrt{2} \times 230$ V and 50 Hz, respectively, according to the local ones. The H-bridges switching frequency, in all converters under test, has been set to 2 kHz. The output-filter inductor has been selected as 3.5 mH. The MPPTs were the conventional perturb and observe type [22], and their voltage increment and frequency have been, respectively, set to 0.5 V and 10 Hz.

B. Test Phases

The proposed converter has been tested during three time intervals as the following. The system starts first operating under the STC until the MPPTs settle down, during which the switches S_{5i} and S_{6i} are turned ON simultaneously to simulate the operation of the CHB. By the end of this phase, at the instant 3.5 s of the test, the converter experiences a sudden decrease in the solar irradiance in the third cell by half for 1.5 s, considering it as a second time interval. Note that, during the second time interval, the switches S_{5i} and S_{6i} were still turned ON simultaneously, emulating the operation of the CHB. At the instant 5 s of the test, the third power cell was still shaded, but the system started operating as a cascaded H6 inverter, where the semiconductor switches S_{5i} and S_{6i} began their normal operation as explained earlier in Section IV.

Fig. 8 shows the three previously described time intervals, where the power extracted from the PV strings and cell voltages are considered. Note that the lines of the power in cells one and two are not clear in Fig. 8(a) since they are congruent with that of the first power cell. Fig. 9 shows the output voltage of the proposed converter as well as the current injected into the grid when it was operating during the first time interval. As it can be seen from Fig. 9, the proposed topology provides similar results to those reported in [6], whose are of the CHB in case of balanced solar insolation.

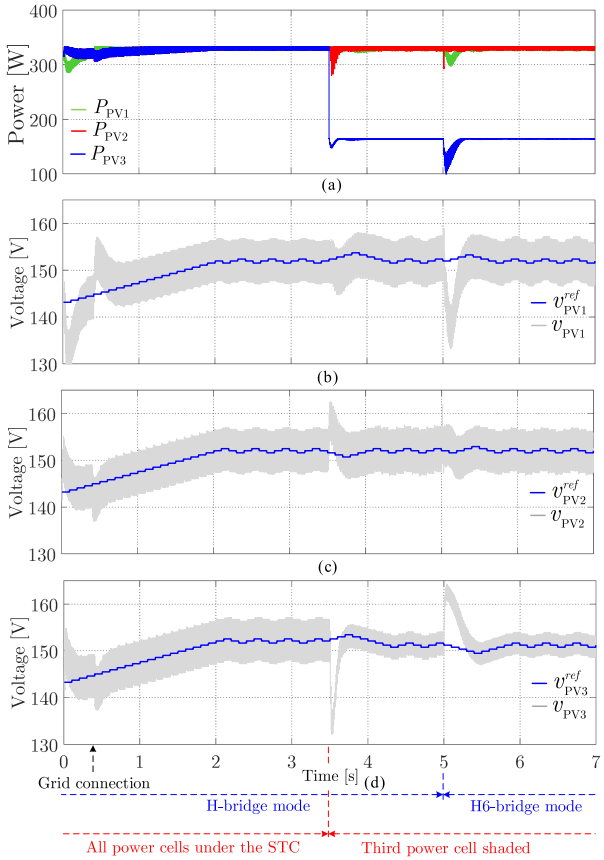

Fig. 8. Simulation results of the proposed topology during balanced and unbalanced solar irradiance. (a) PV powers. (b) Reference and measured voltages of the first PV string. (c) Reference and measured voltages of the second PV string. (d) Reference and measured voltages of the third PV string.

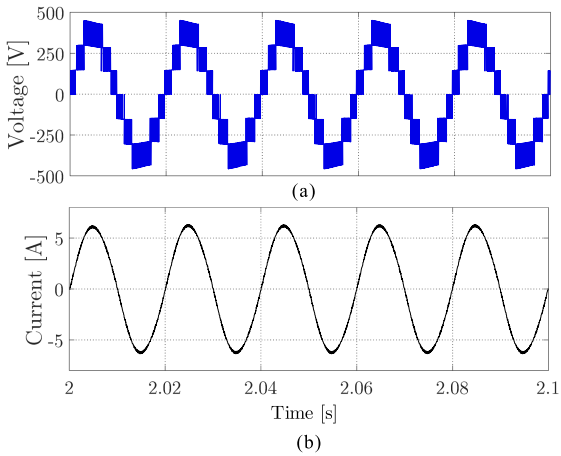

Fig. 9. (a) Output voltage and (b) grid current, when the three PV strings of the proposed topology are under the STCs.

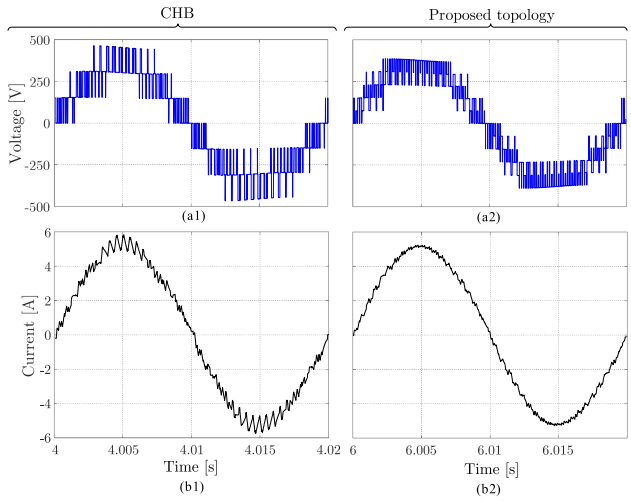

Fig. 10. Output voltage and current injected to the grid of both the CHB and proposed topology when the first and second cells are subjected to 1 kW/m^2, whereas the irradiance of the third cell is 0.5 kW/m^2.

The output voltage and injected current of the seven-level CHB, during the second time interval, are, respectively, shown in Fig. 10(a1) and (b1). One can note from Fig. 10(b1) that the injected current to the grid has a ringing around the peak area. Fig. 11(a) and (b) shows the harmonic spectrums of the CHB's output voltage and current during this time interval. As it can be seen from these two harmonic spectrums, the voltage and current distortions are due to high-order harmonics, which are located at the switching frequency and its multiple ($2f_{sw}$). In order to inject power to the grid, there are grid codes and requirements by the grid operators, which need to be respected and could be on the converter's output current, voltage, or both. Table II lists the total harmonic distortion (THD) calculated up to the 30th, 50th, and 100th harmonic orders for both converter output voltages and currents, and considering the three test time intervals, i.e., balanced CHB, unbalanced CHB, and unbalanced cascaded H6. From this table, it can be seen that the CHB failed to comply with current distortion limit according to the IEEE 514-1992,

TABLE II
OBTAINED THD CONSIDERING THE HARMONICS UP TO THE 30TH, 50TH, AND 100TH ORDERS IN THE OUTPUT VOLTAGE AND GRID CURRENT

		Up to the 30th order			Up to the 50th order			Up to the 100rd order		
THD (%)	Output voltage	2.11	2.12	2.11	2.18	14.86	10.42	2.24	21.89	12.25
	Grid current	2.11	2.11	2.11	2.18	6.28	4.25	2.24	9.88	4.92

Balanced CHB | Unbalanced CHB | Unbalanced Proposed topology

as it reached 6.28%, which is above 5%. On the voltage side, it also failed to comply with both IEEE 514-1992 and EN50160 [23], as the THD reached 14.86% and some individual high-order harmonics reached even 6.5%, as shown in Table II and Fig. 11(a).

Fig. 12 displays the cell duty cycles during the transition between the second interval and the third time interval of the test. As can be seen from this figure, the duty cycle of the third cell during the second time interval has a peak value that is nearly half of the peaks of the duty cycles in cells one and two. As a result, the third cell is operating less than the rest of cells—during each switching interval, the third power cell starts after a delay and stops in advance, as explained in Section II. One should note from Fig. 12 that, as the third time interval started, where the converter began to operate as proposed, the peak of the duty cycle of the shaded cell increased and ended up reaching nearly the unity after 0.2 s. The reason of the increased duty cycle lies on the fact that the instantaneous delivered power by the cell has been reduced by half since its voltage seen by the output of the converter has been reduced by half. Under these circumstances, the total cell voltage has increased above its reference as shown in Fig. 8(d), which caused the controller to increase the duty cycle in order to decrease the PV voltage back to its reference.

It can also be noted from Fig. 12 that the duty cycle of the first cell got affected since it is designated for the control of both the total and first cell voltages. The modulation index of the first cell settled down again after 0.2 s.

As it can be observed from Fig. 10(b2), the current provided by the proposed topology does not present any ringing since the duty cycle peak in the shaded cell has nearly reached the unity. From Table II, it can be seen that the current THD complies with the described limit by the IEEE 514-1992, as it has been improved to 4.25%. Regarding the voltage, although the THD has been decreased from 14.86% to 10.42% by the proposed topology, some individual high-order harmonics still overpass the described limits by the EN50160, as shown in Fig. 13(a). Accordingly, in case the voltage is examined, the output filter needs to be increased in a way the remaining individual high-order harmonics are compensated.

C. *Efficiency*

For evaluating the efficiency of the proposed topology, one of the possible solutions offering harmonics performance improvement during partial shading, namely the CHBB (see Fig. 1) is also considered.

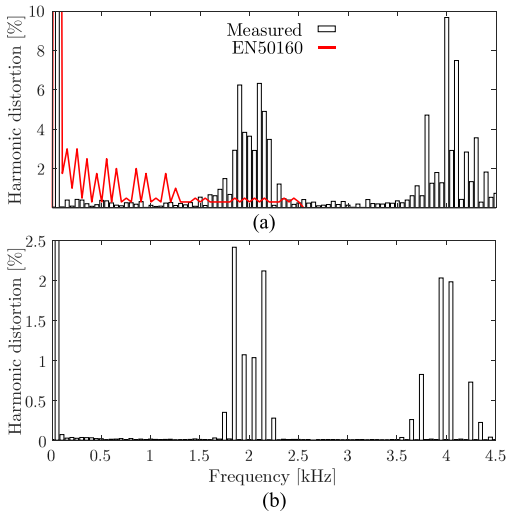

Fig. 11. (a) Harmonic spectrum of the CHB's output voltage. (b) Current injected to the grid, under an unbalanced solar irradiance condition.

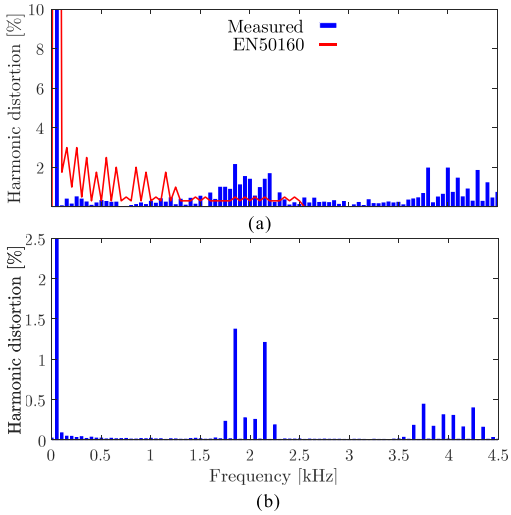

Fig. 13. (a) Harmonic spectrum of the proposed topology's output voltage. (b) Current injected to the grid, under the unbalanced solar irradiance condition.

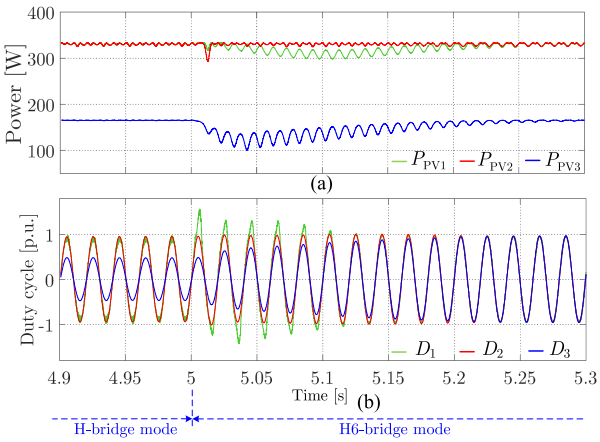

Fig. 12. Duty cycles of the three cells when the converter is operating first in the H-bridge mode and then in the H6 mode. The first and second cells are under the STC, whereas the third one is under 0.5 kW/m^2.

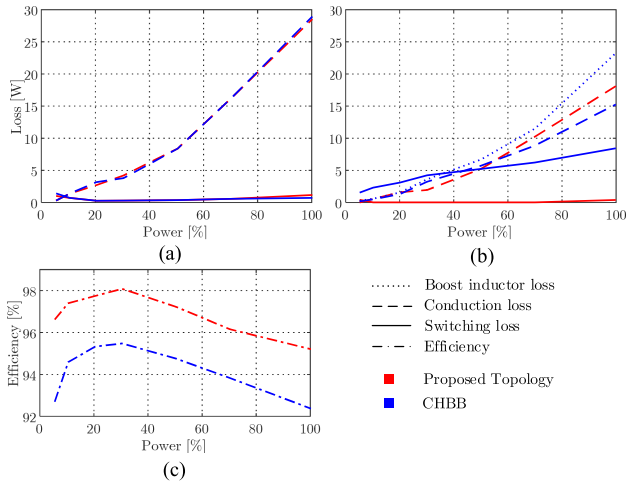

Fig. 14. Loss of (a) H-bridges, (b) dc–dc boost stages and added elements in the proposed topology ($S_{5,6}$, $D_{5,6}$), and (c) resulted overall efficiencies.

For assessing the thermal loss, the semiconductor devices have been thermally modeled according to their real datasheets. For the IGBTs, the FGPF30N30 semiconductor devices were used, whereas for the diodes, DPG30I300PA were the employed ones. On the dc–dc boost stages, the inductors have been designed in a away 20 kHz switching frequency should be applied in order to obtain a 25% current ripple. Note that the loss in the converters' output filter have been neglected for both tested topologies.

The switching and conduction losses of the H-bridges in both the CHBB and proposed topology are shown in Fig. 14(a). Those of the dc–dc boost stages in CHBB and added elements in the proposed topology ($S_{5,6}$, $D_{5,6}$) are shown in Fig. 14(b). The dc–dc boost inductor losses are also shown in the latter. As it can be seen from Fig. 14(a), the H-bridges of both converters have equivalent switching and conduction losses since the power harvested, components count and type, and switching frequency are all the same. On the dc–dc boost stages in the CHBB and $S_{5,6}$ and $D_{5,6}$ in the proposed topology, the conduction losses are still equivalent; however, on the switching loss, significant differences can be observed, the proposed topology being the one having the least. Moreover, the dc–dc boost inductors loss are quite significant, where they can be estimated to reach as twice as the switching loss in the high power range.

One can note from Fig. 14(c) that these loss differences have caused the proposed topology to reach higher conversion efficiency over the CHBB topology in the whole power range. The top efficiency registered by the CHBB was 95.45%, whereas the proposed topology reached 98.07%. The European efficiency [24] has been calculated, respectively, as 94.32% and 96.96%, for the CHBB and the proposed topology.

VII. Experimental Results

To validate both the theoretical analysis and obtained results by simulation, an experimental prototype of the proposed

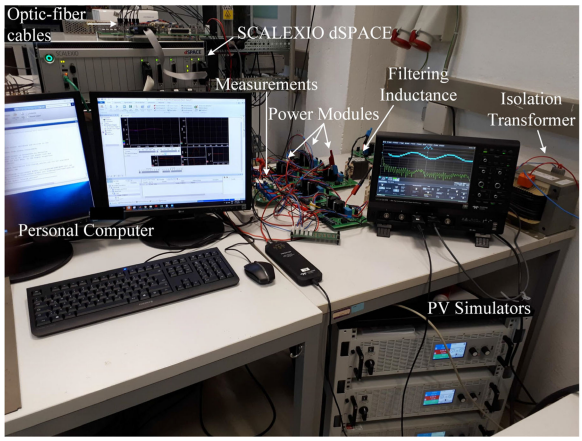

Fig. 15. Experimental test bench used to validate the proposed cascaded H6 inverter for PV applications.

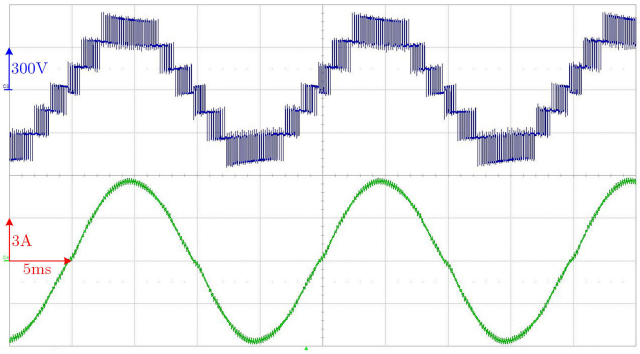

Fig. 16. Output voltage and current injected to the grid of the proposed topology under the balanced operation.

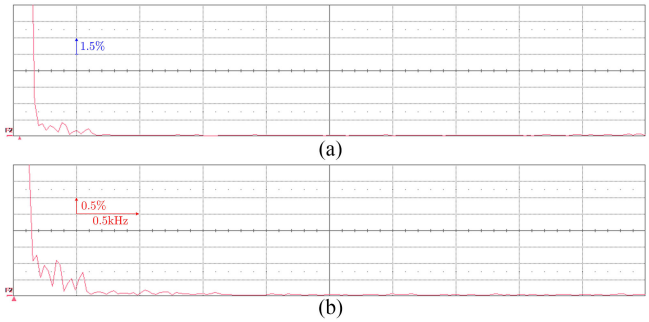

Fig. 17. Harmonics spectrum of conventional CHB under the balanced operation in (a) output voltage and (b) current injected to the grid.

topology has been built. The overall test bench for testing the proposed converter is shown in Fig. 15, which consists of custom-made power modules forming the built prototype, three ELEKTRO-AUTOMATIK PSI 91500-30 PV emulators for simulating real PV curves, dSPACE SCALEXIO for running the control algorithm, isolation transformer to galvanically isolate the grid from the power circuit prototype, and voltage and current measurement sensors. Note that the same PV model, switching frequency, cell capacitors, grid voltage and frequency, and output filter specifications described in the simulation section are also used here. The control algorithm is implemented on the DS6001 digital processing board, which sends the control signals to the DS2655M2 field programmable gate array (FPGA), with an update rate according to the aforementioned switching frequency. The developed modulation strategy, which is explained in Section IV, has been programed in DS2655M2 FPGA, with a resolution of 8 ns. The outputs of this board are converted from electrical digital to optic digital, and are transferred to the power stage through fiber-optic cables to eliminate possible electromagnetic coupling. The voltage and current analogic measurements are transferred to the DS6001 digital processing board through DS6221 analogic to digital conversion board for a high resolution.

The same tests procedure, which was performed in the simulation, has been followed here as well. Fig. 16 shows the proposed converter's output voltage and current injected to the grid during the balanced operation. As it can be seen from this figure, the proposed converter has a seven-level output voltage waveform similar to the one of the conventional CHB with three cells. According to Fig. 17, which depicts the harmonics spectrums of both the output voltage and current injected to the grid, the high-order harmonics are less than the low-order ones and are negligible. Accordingly, the voltage THD calculated up to the 30th harmonic order and up to the 50th one increases only from 3.64% to 4.68%.

Fig. 18 shows the output voltage and current of the proposed converter when one of the cells is shaded, whereas the switches S_{5i} and S_{6i} were forced ON, emulating the behavior of the classical CHB. One can see from the output voltage that it is distorted and from the current injected to the grid that it suffers from a severe ringing around the peak area where the difference in the duty cycles becomes prominent. Consequently, both the output voltage and current suffer from high-order harmonics situated at the switching frequency and its multiple, as it is depicted by the harmonic spectrums in Fig. 19. The voltage THD has been calculated according to the EN50160 standard as 15.23%.

As one can see from Fig. 20, which shows the output voltage and current of the proposed converter when the switches S_{5i} and S_{6i} began their operation as explained in Section IV, the voltage waveform has been improved and the ringing in the current

injected to the grid has been significantly reduced. Accordingly, the harmonics performance of the PV-fed MLC have been greatly improved as indicated by the red arrows in the harmonics spectrums in Fig. 21, yielding to a voltage THD, according to EN501650, of 10.75%.

VIII. Conclusion

The key reasons behind the output current and voltage distortions in cascaded MLCs, in the presence of partial shading among the power cells, were analyzed in this article. It was demonstrated that both the difference in cell duty cycles as well

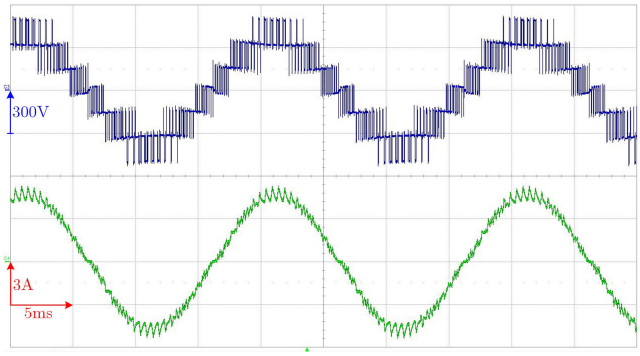

Fig. 18. Output voltage and current injected to the grid of the conventional CHB when the third cell is shaded.

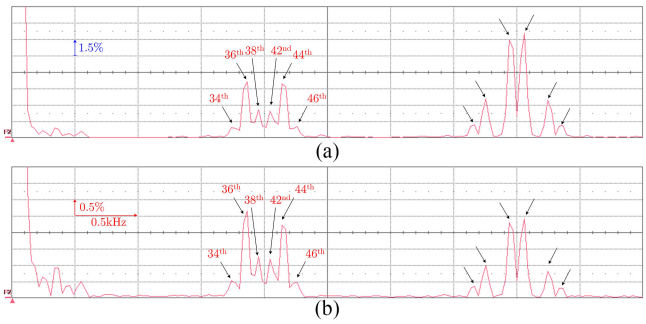

Fig. 19. Harmonics spectrum of the conventional CHB when the third cell is shaded in (a) output voltage and (b) current injected to the grid.

as their voltages were the main factors in the distortion of these output signals. Moreover, the difference in cell voltages could have a less effect, in this matter, if the cell duty cycles were close the unity. Accordingly, a cascaded MLC was proposed, where the cells were able to provide less voltage than the total cell one, which, in turn, allows the cell duty cycle to be raised back to unity after it decreases in case of partial shading. The proposal was cost effective, lighter, and less sizable since it did not require extra passive elements with respect to its counterparts. Only some active components were added. The proposed converter was tested under both simulation and experiment, and it was shown that it provided a significantly improved output voltage and current qualities in case of partial shading, where the THD according to 50th harmonic orders–as included in the EN50160 standard–was decreased from 15.23% to 10.75% in the voltage.

Furthermore, a loss and efficiency comparison with respect to its counterpart CHBB was included in this article. Due to the employment of the same switching frequency as in the CHB in the proposed converter, it suffered from less switching loss compared to the CHBB. Moreover, the proposed converter did not employ any inductors in the cells, evading more loss. Consequently, the proposed converter registered a European efficiency of 96.96%, showing an improvement of the 2.64%.

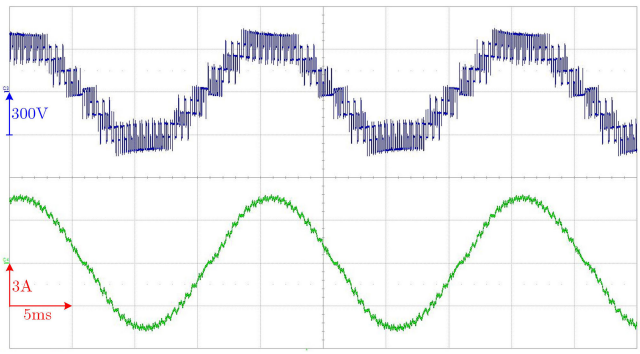

Fig. 20. Output voltage and current injected to the proposed topology when the third cell is shaded.

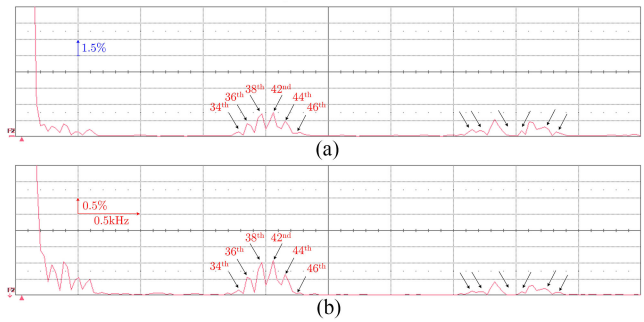

Fig. 21. Harmonics spectrum of the proposed topology when the third cell is shaded in (a) output voltage and (b) current injected to the grid.

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